

# Itanium 2 Platform and Technologies



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# Intel's Itanium platform

- **Top 500 lists:** Intel leads with **84 Itanium® 2-based systems**
- Continued growth in MSS: Itanium processors
- RISC to Itanium migration – enterprise and HPC

## RISC and IA Server System Revenue MSS

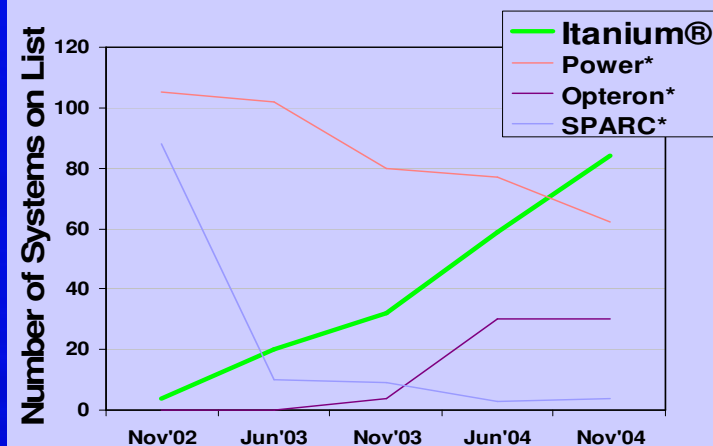
*First time to pass RISC*



Source: IDC Server Tracker Q4 '03

## Systems in HPC Top500 by Architecture

*First time to pass top RISC arch*



# Commitment to Itanium® Architecture

- ✓ 4 generations of Itanium® 2-based products in definition and development
- ✓ >1200 Intel software engineers working on Itanium 2-based tools, compilers, and ecosystem
- ✓ >5000 certified applications available
- ✓ Excellent support of x86 applications with IA-32 Execution Layer technology



***Heavy investment reflects deep commitment***



# Itanium® Architecture Positioning

Focused on the applications typically served by RISC, targeting:

- General RISC migration (2-512P+)
- Large SMP/mainframe-class
- High performance computing (HPC)



## Leading capabilities in Intel's server product line

- **Higher performance & scalability driven by core architectural differences, e.g.**
  - EPIC technology
  - Massive on die resources
  - True 64-bit addressability
- **Greater RAS capabilities**
  - Designed for 99.999%+ uptime
  - Machine Check Architecture, bad data containment, cache reliability,...
- **Offered in high end systems from leading enterprise hardware vendors**
  - HP\* 2 - 128P 256\*



## Cost effective alternative to proprietary RISC

- **Outstanding price/performance<sup>1</sup>**
  - Top TPC-C performance on Linux\*, Windows\*, HP-UX\*, Oracle\*, & SQL\*
  - 30% better \$/tpmC than RISC<sup>1</sup>
  - *Huge* advance in performance & platform features coming on Montecito
- **Greater choice**
  - System vendors
  - Operating systems
  - Software applications
  - Continued strong ecosystem growth

***Focused on replacing RISC, complementary to Intel® Xeon™ processor***



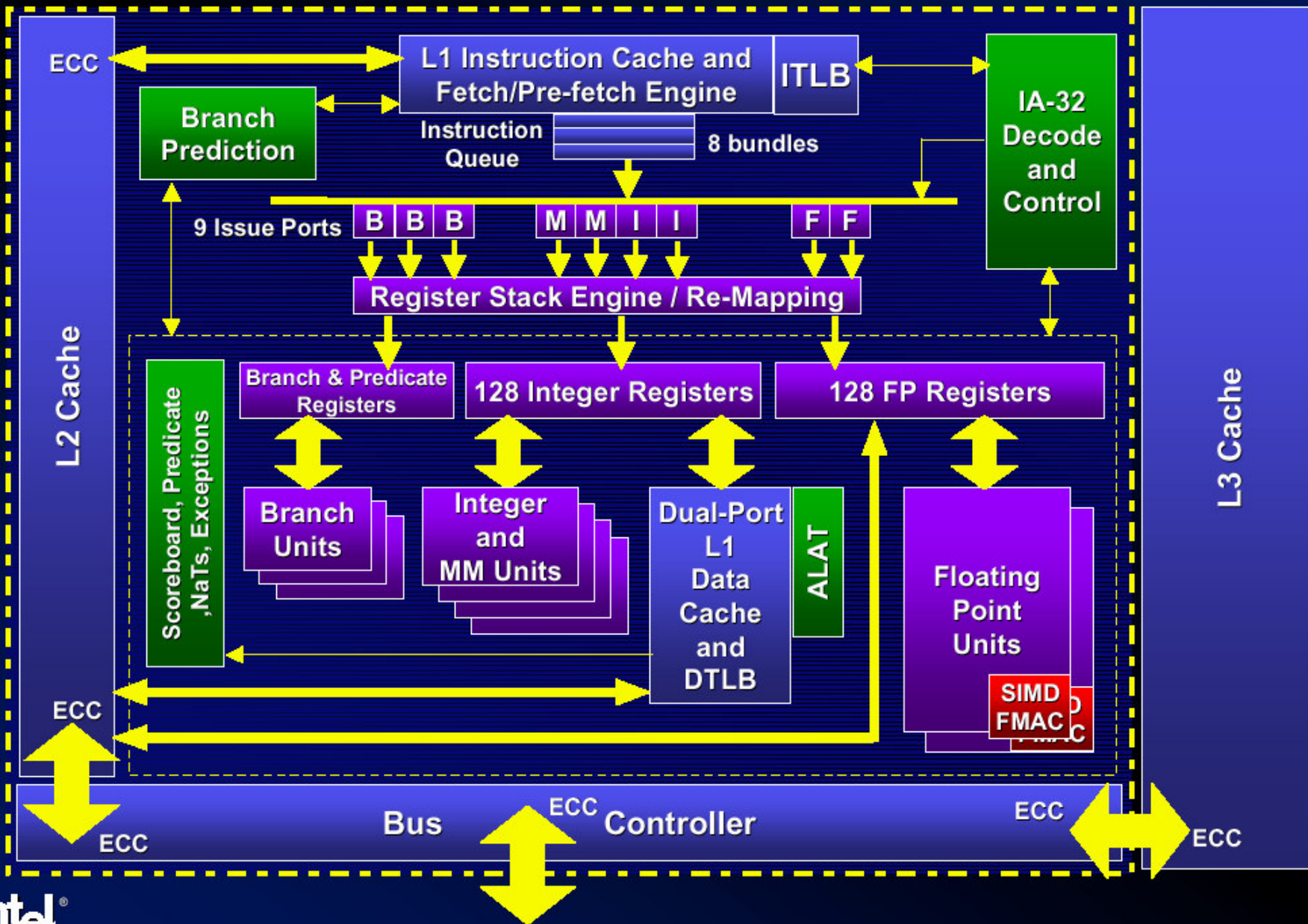
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details

# Intel® Itanium™ Processor Block Diagram



# 64-Bit Addressing – How big is it?

## 32-bit Addressing

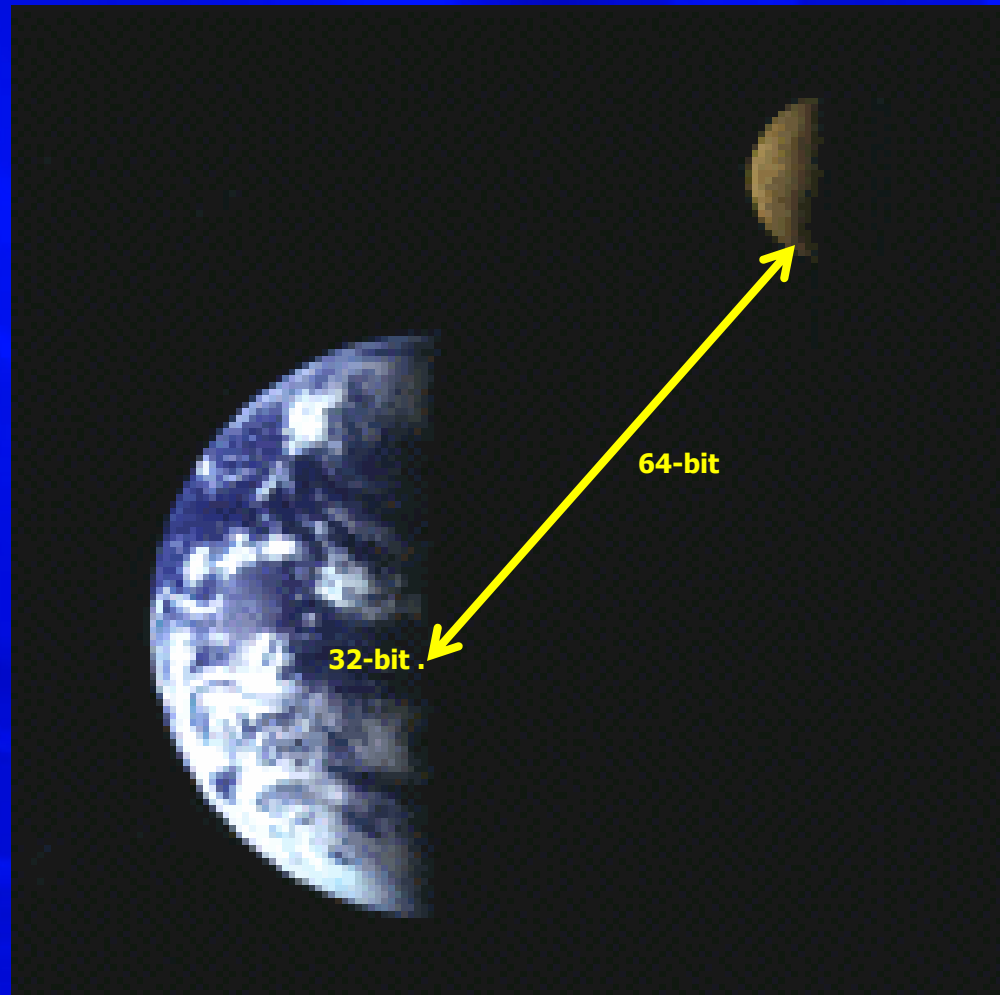
- 1 cm
- one CD cover height

## 64-bit Addressing

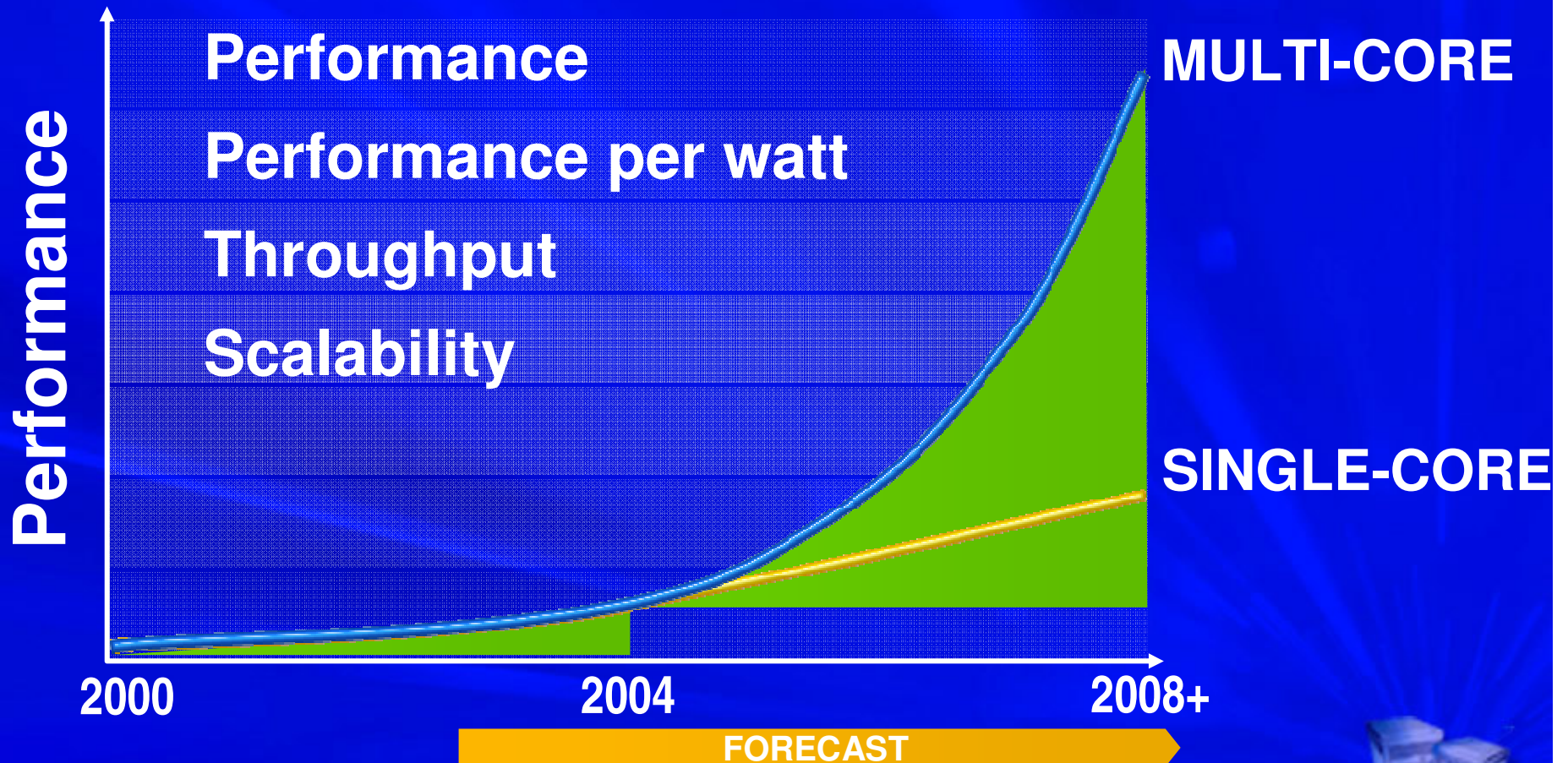
- 429496 km
- distance between Earth and Moon

$$2^{32} = 4,294,967,296$$

$$2^{64} = 18,446,744,073,709,551,616$$



# Parallelism



*An Industry Inflection Point*

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# Long Term Goal: 1M Transactions per Minute <sup>A</sup>

Today

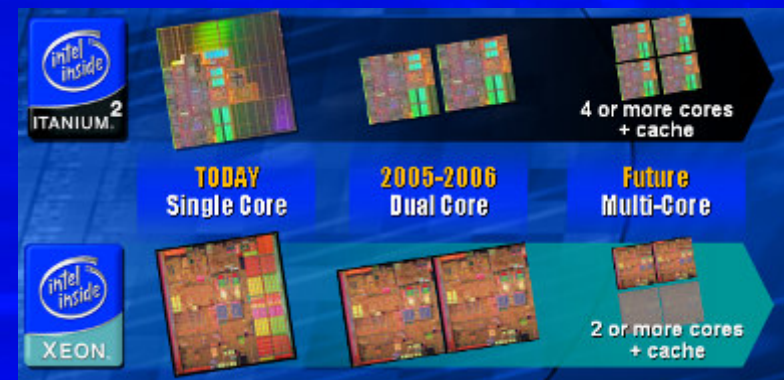


In 2007



With planned performance improvements, a 4-way Itanium®-based server in '07 could deliver equivalent OLTP of a current 64-way system, delivering dramatically

- Lower TCO
- Lower power consumption
- Higher density



Shown are representations of 64-way system (today) and 4-way system (2007). Not to scale.



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# Itanium® Architecture Innovations

## 2004 & Prior Enhancements

EPIC architecture  
Enhanced Machine Check Architecture  
FMAC for floating-point leadership  
Largest on-die resources for demanding workloads



## 2005 Planned Enhancements

Dual-core; Multi-threading  
Virtualization  
Dynamic Performance Boost (Foxton)  
Demand Based Switching (DBS)  
PCI Express, DDR II  
Enhanced System Bus Bandwidth, cache reliability, and processor performance

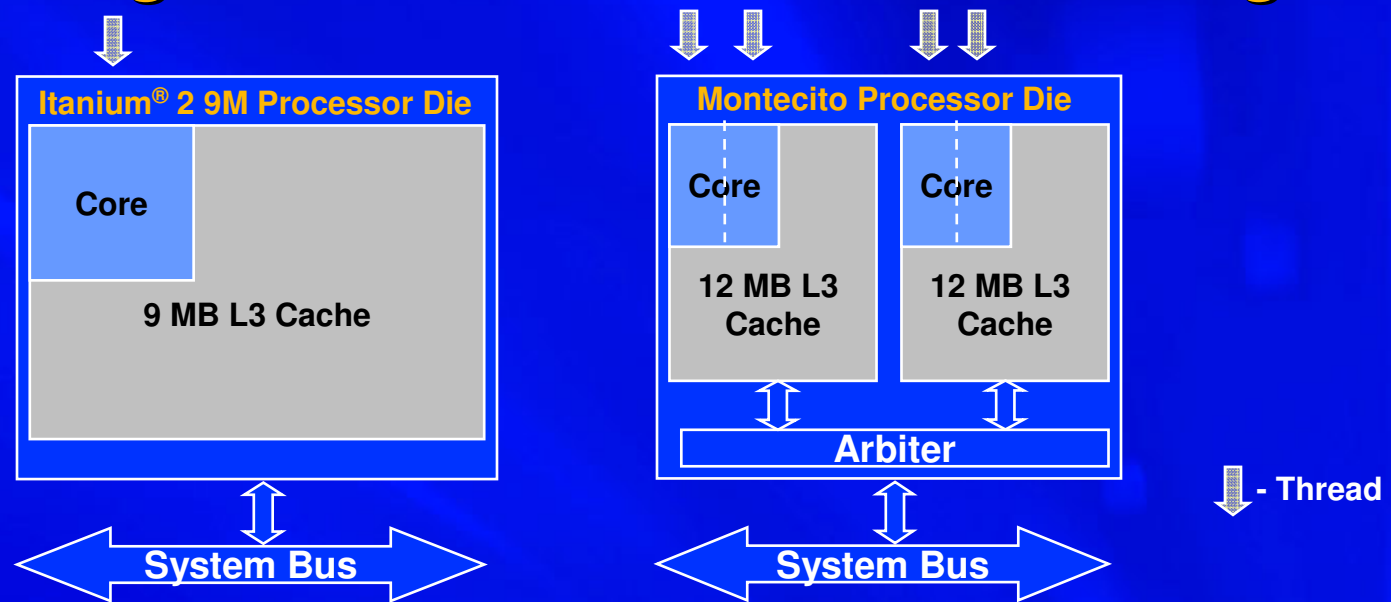
## Future Enhancements

Common platform architecture with Intel® Xeon™ processor family  
Multi-core  
Enhanced Virtualization  
Enhanced I/O, memory & RAS

***Innovations deliver Intel's highest performance, reliability and scalability solutions for the enterprise***



# Introducing Dual-Core and Multi-Threading



- **Dual-Core**
  - 2 Processor cores per physical package each with independent L3 cache
- **Multi-Threading Technology**
  - 2 Threads active per Core (4 per Socket)
  - High CPU utilization for multithreaded server applications

**Montecito hardware-enhanced thread-level parallelism  
with 2 cores in a single package**

# Montecito Status

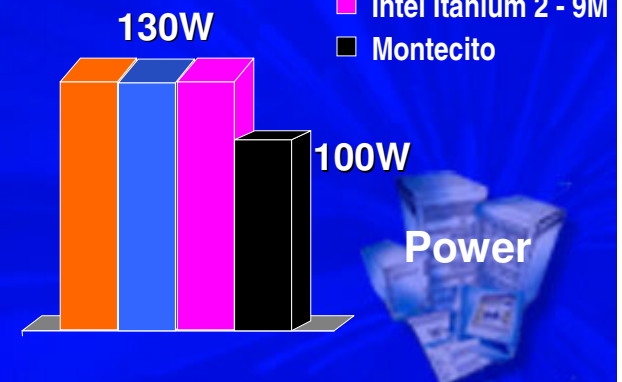
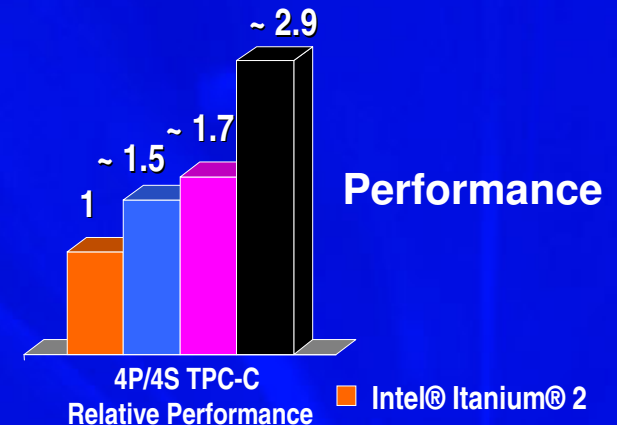
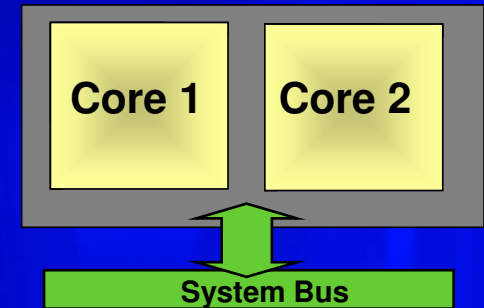
- **Montecito: Next Itanium® Processor Family product after Madison-9M**

- Dual core, Multi-threading, 24MB cache
- Platform compatible with Itanium® 2 processor
- First 1.72 billion transistors processor
- Significant performance jump with lower power
  - 1.5-2x over Madison-9M
  - 100W
- Demo'd last year, first samples were in Sept'04
- OEMs currently testing Montecito platforms
- Seeding programs
- Montecito shipping in 1H 2006

- **Montecito also brings new technologies**

- **Foxton: Performance boost while maintaining power**
- Multi-threading
- Vanderpool: Virtualization
- Reliability with Pellston, more hardware error correction
- **Demand Based Switching: Server power savings**

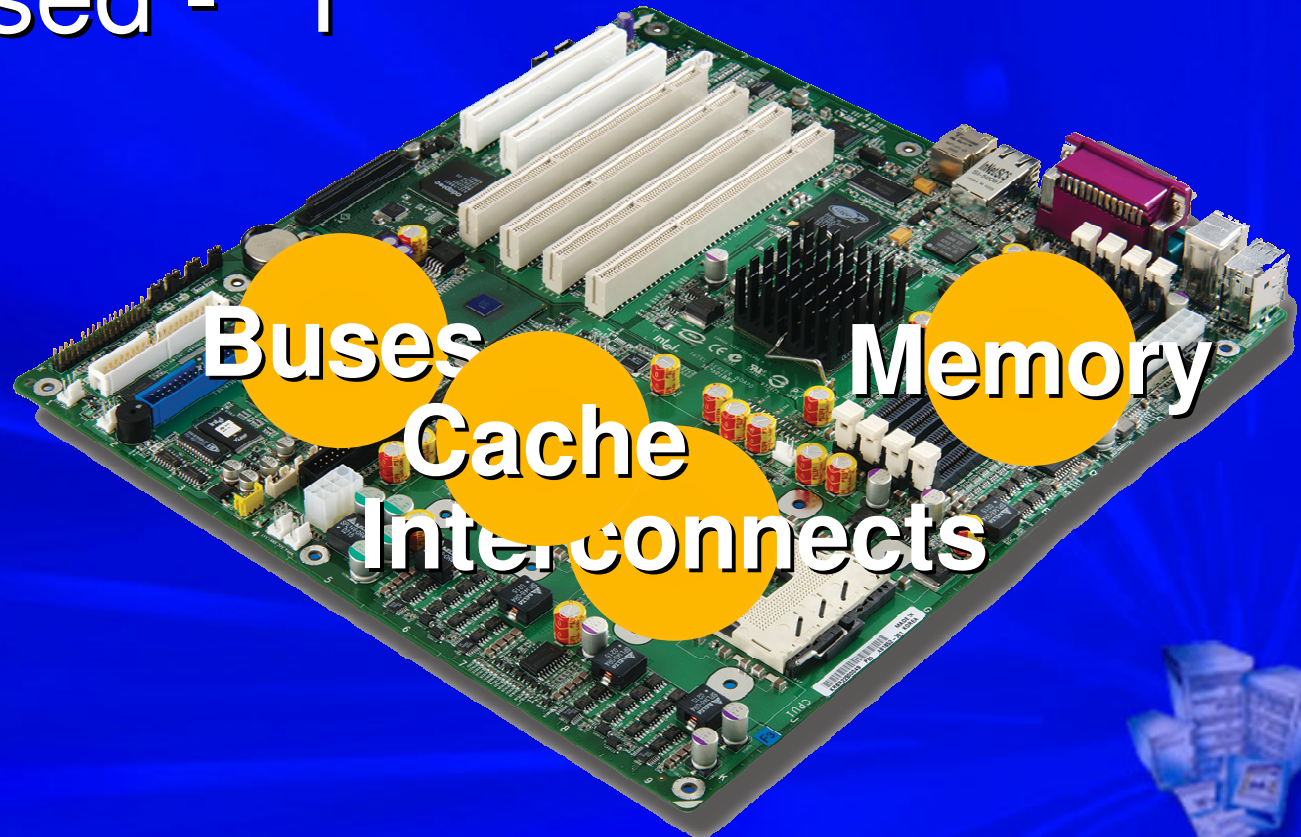
Montecito



# A New Architectural Approach

Platform

Focused - \*T

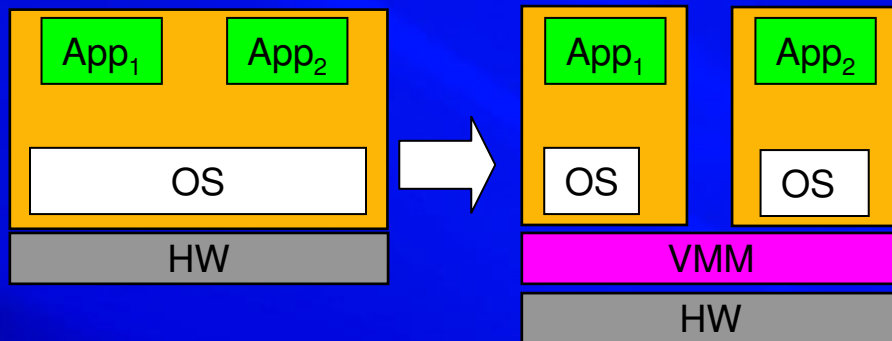


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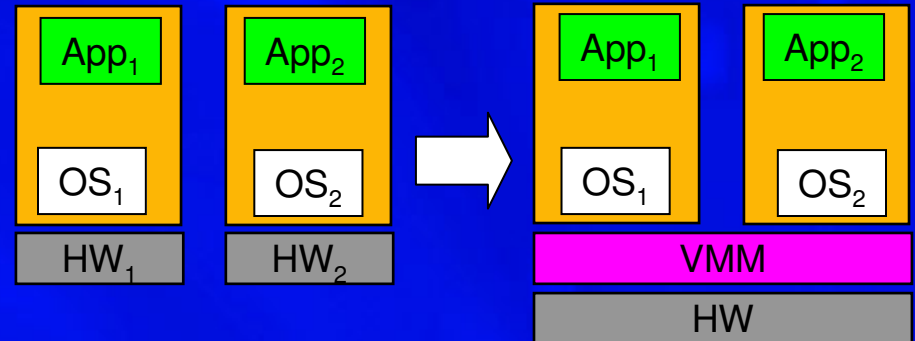
# Virtualization Usage Models

Enables running separate production and development environments on same server

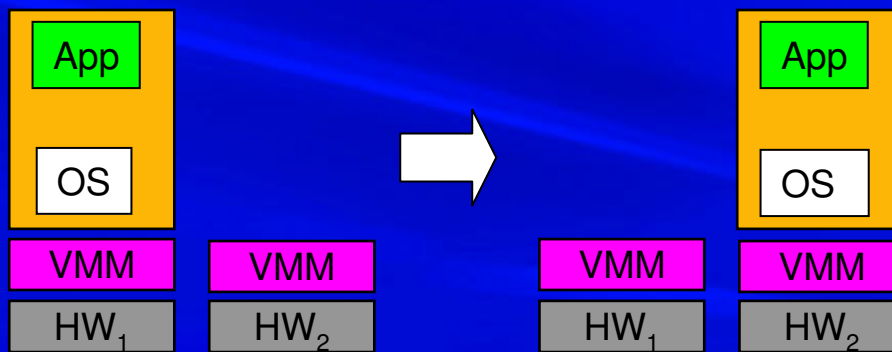
## Workload Isolation



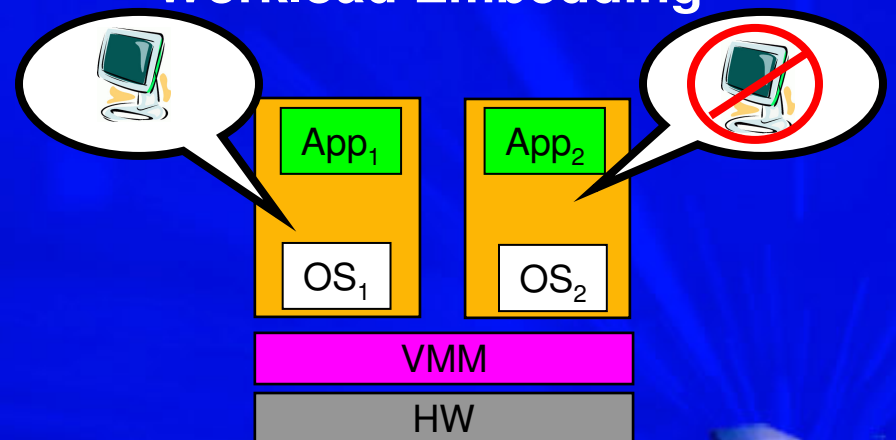
## Workload Consolidation



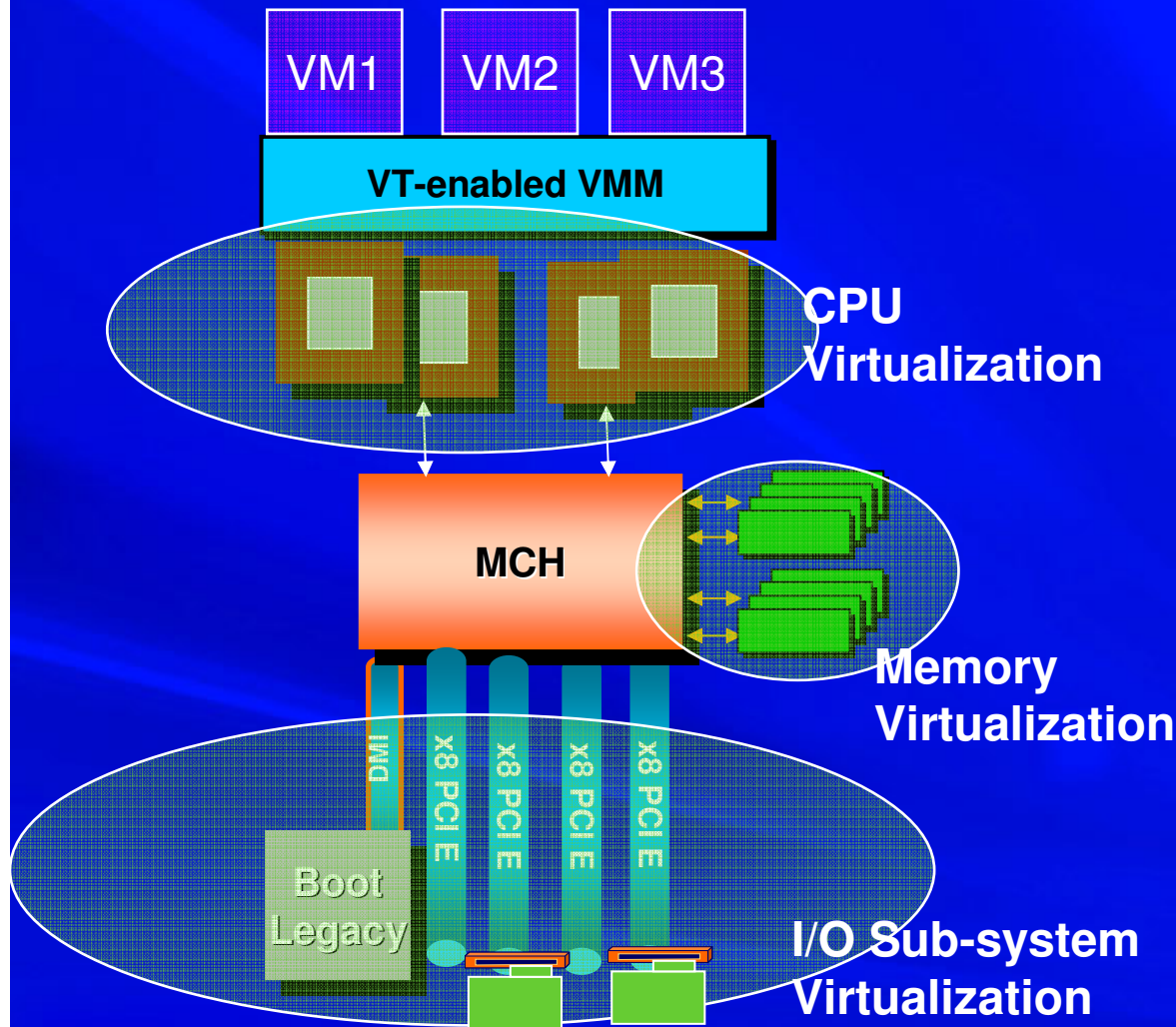
## Workload Migration



## Workload Embedding



# Advantage of HW virtualization



## *Dramatic Benefits Expected*

### Increased Robustness

- Reduced Complexity
- Minimizing SW conflict

### Improved Flexibility

- Simplify VMM development
- Standard interfaces
- Support legacy environment

### Enhanced Functionality

- Support for latest HW capability

### Better Performance

- Reduce emulation overhead
- Access to physical resource

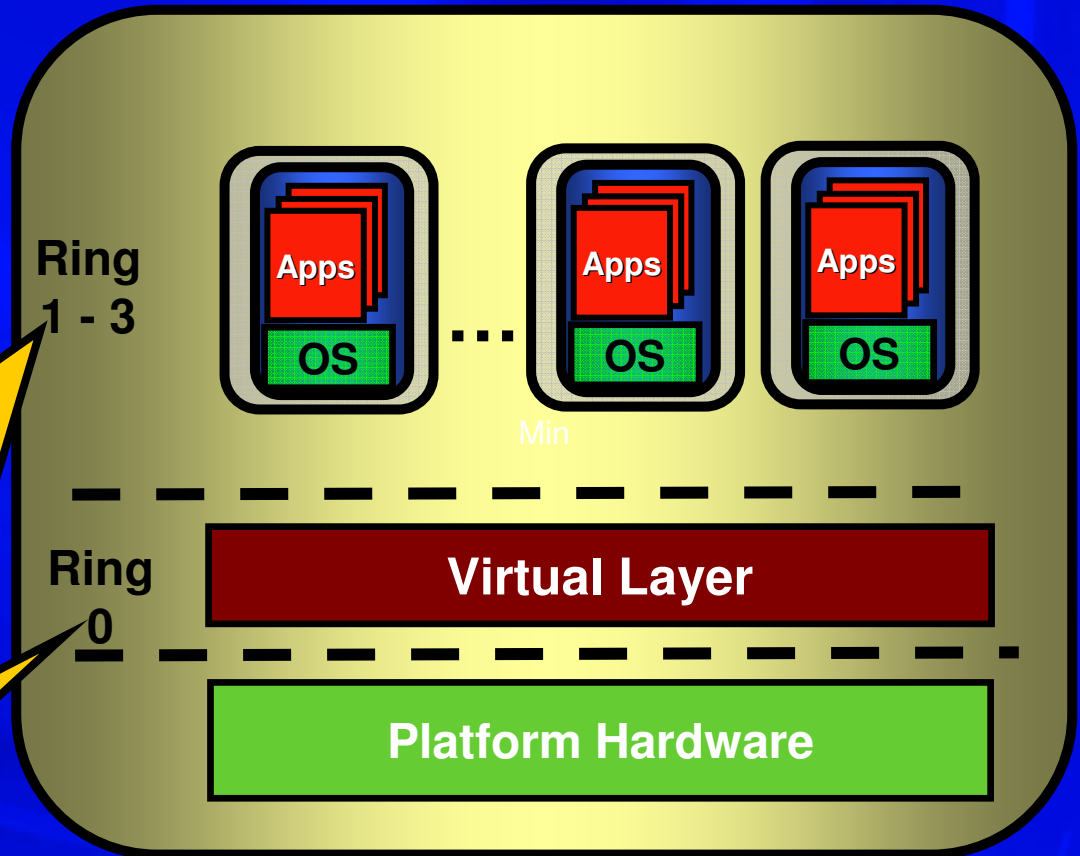


**Intel driving virtualization technology across all server platforms**

# Virtualization Issues

- Virtualized OS's "De-Privileged"
- Ring-0 code run in Rings 1-3
- Results in:
  - Excessive faulting
  - Ring compression
  - Manageability and stability issues

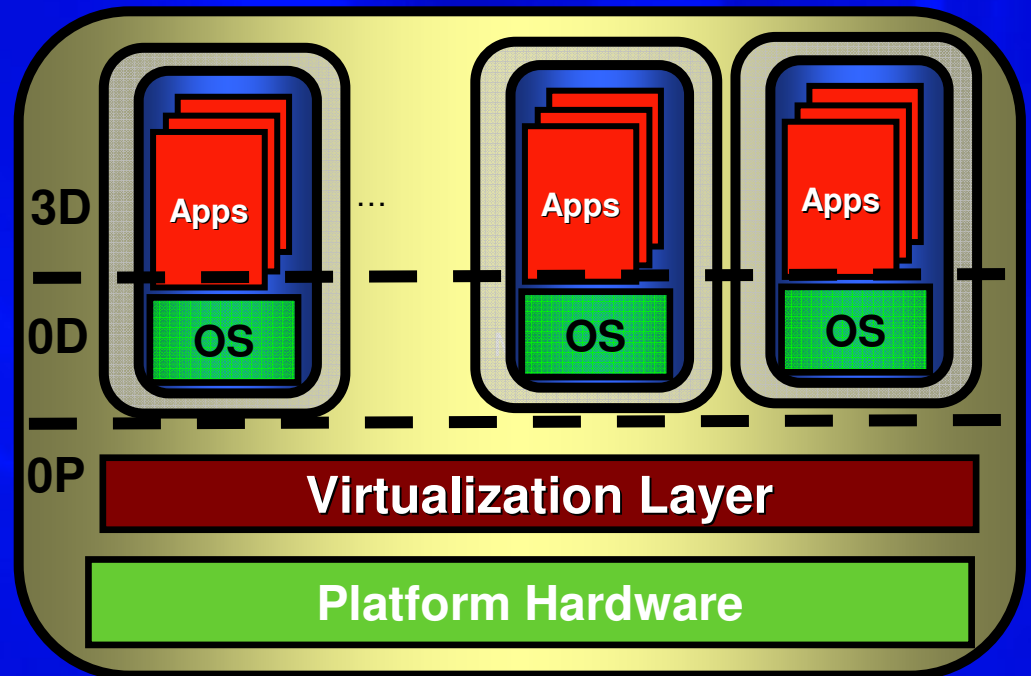
- Virtualization SW operates in Ring-0
- Traditional OS domain



Virtualization SW uses a combination of emulation, dynamic patching, and binary translation to work around these problems

# - Virtualization Extensions

- **New CPU execution mode**
  - OS's run at expected privilege levels
  - Enables new privilege level (0P) for Monitor
- **HW-based mode transition**
  - Programmable VM transition triggers to streamline process
  - Excessive trapping eliminated by design
  - Address compression eliminated by design
- **New instructions to support entry, exit, configuration and maintenance**
- **Memory protection within the CPU**

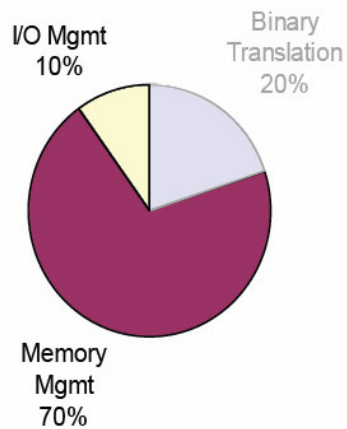




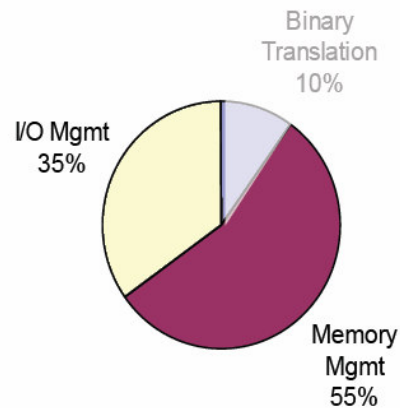
# Current Overhead

Typical percentage of virtualization overheads associated with binary translation, memory and I/O virtualization

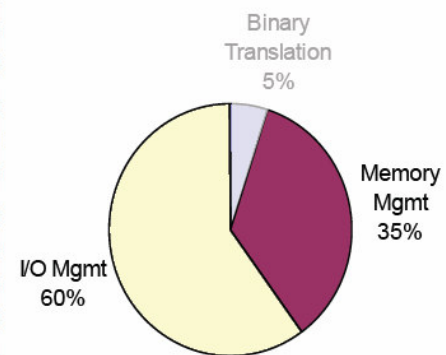
## CPU-based workloads



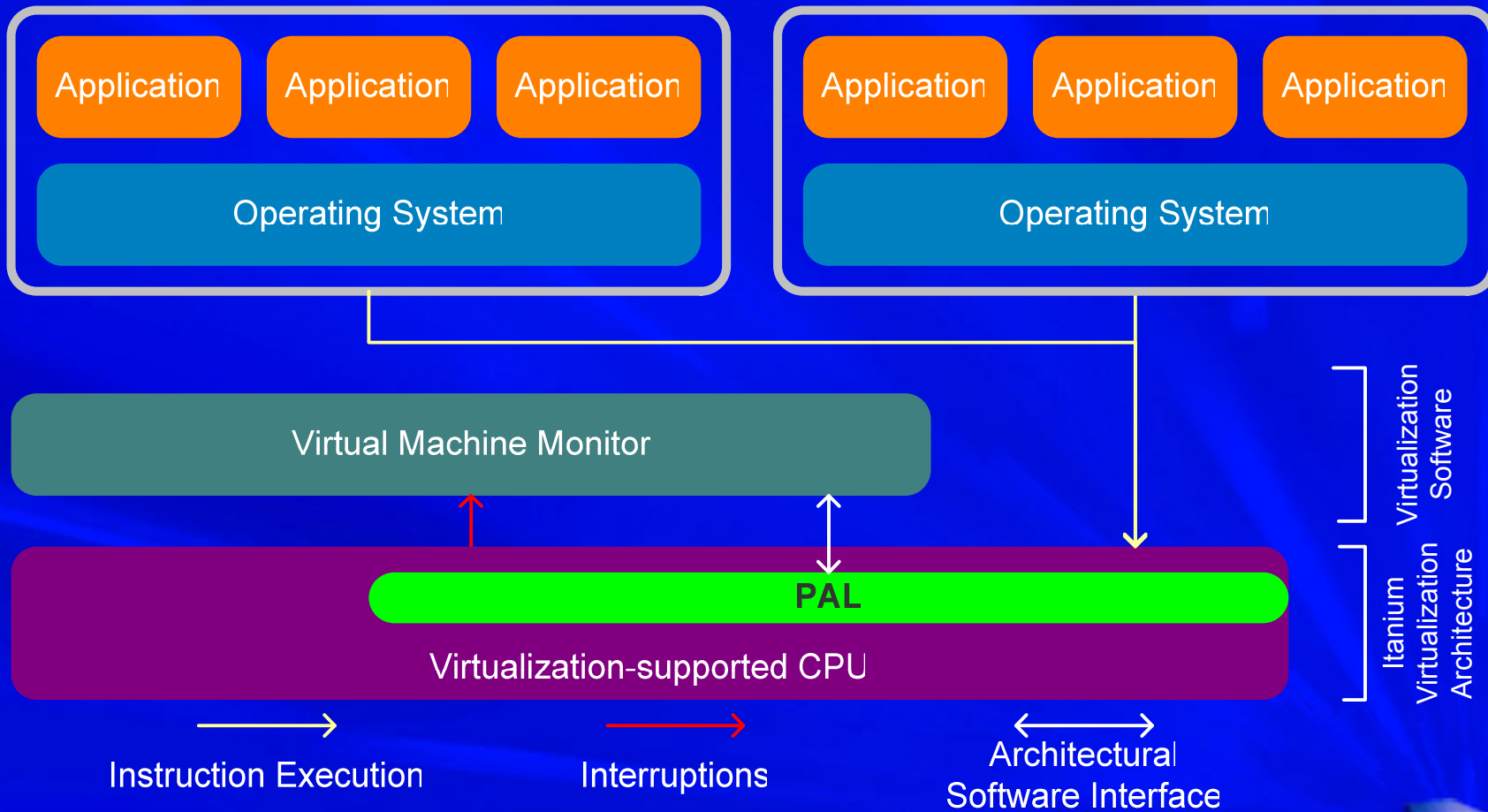
## Mixed workloads



## I/O intensive workloads



# Itanium Virtualization Technology



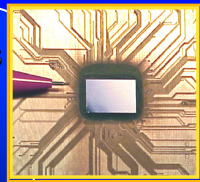
Multiple guest OSes on a single processor

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# Intel's Comprehensive Approach to Power Management

## Silicon Advances

- Process technologies
- Materials
- Circuit design
- Microarchitecture
- Packaging



## Intel Power Tools

- Demand Based Switching
- Power Calculator
- Power Monitor
- Datacenter Framework

## Platform & Architectural Advances

- Multi-core Processors
- Hyper-Threading Technology
- Low power/high speed memory
- Platform/architectural flexibility
- Enhanced Utilization (virtualization)
- Software Optimization

## Whitepaper

[http://www.intel.com/business/bss/infrastructure/enterprise/power\\_thermal.pdf](http://www.intel.com/business/bss/infrastructure/enterprise/power_thermal.pdf)

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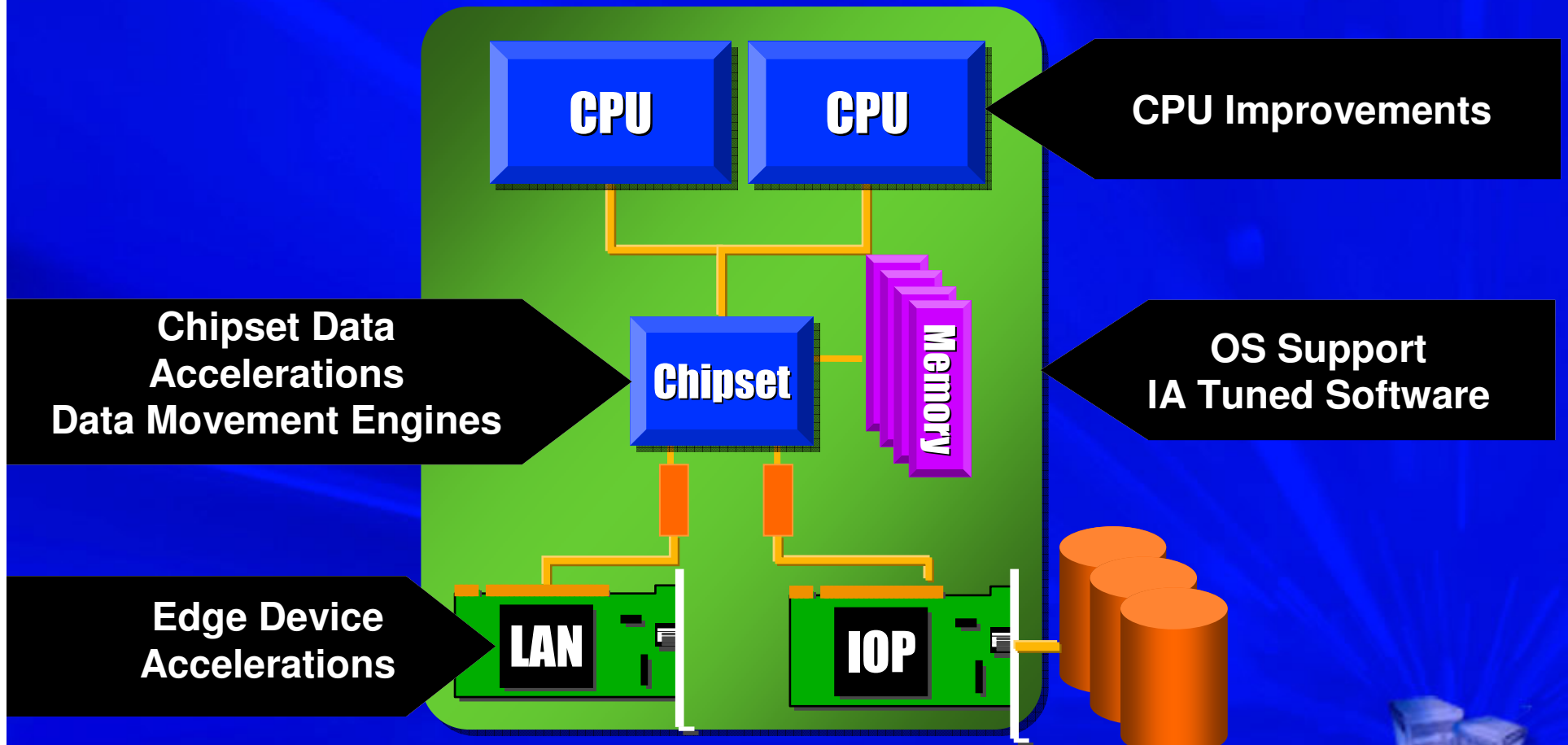


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# Future Technology: Intel® I/O Acceleration Technology



# PCI Express\* Technology Overview



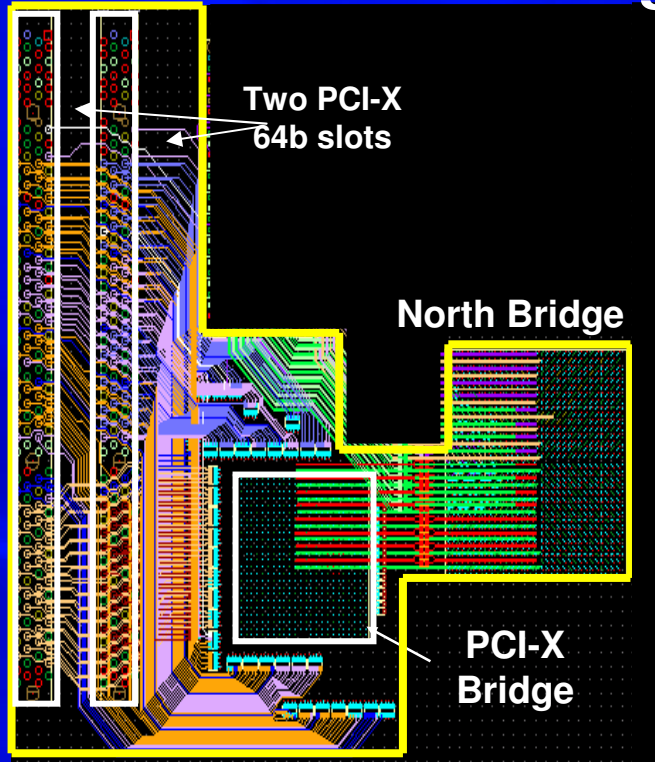
- A PCI Express\* “lane” are four wires
  - One differential pair for transmit and another pair for receive
  - Signaling is at 2.5 GHz with 8b/10b encoding
- Connectors are defined for x1, x4, x8, x16 lanes providing an opportunity to scale bandwidth

Lanes	Bandwidth (peak)
x1	500 MB/s
x4	2 GB/s
x8	4 GB/s
x16	8 GB/s

# Improves Board Cost

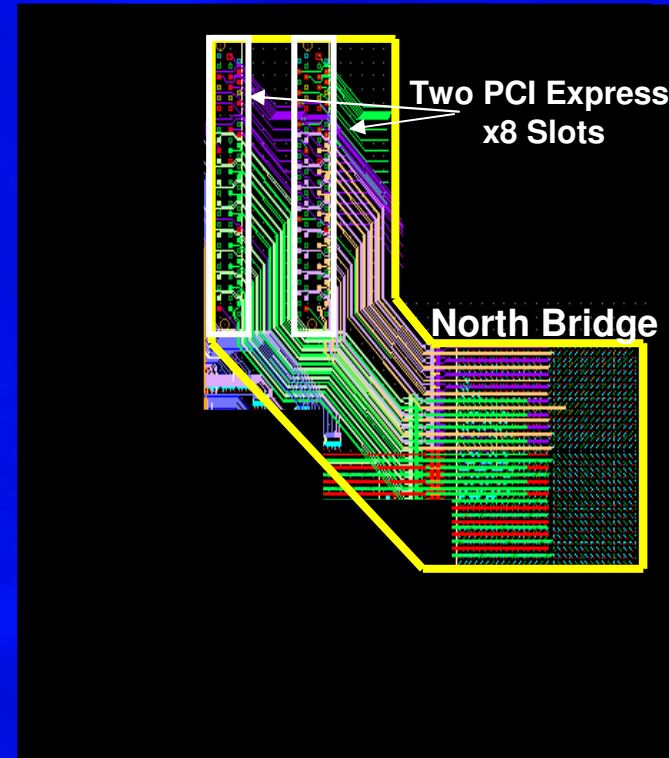
PCI-X:

Two 64b Slots & Bridge



PCI Express\*:

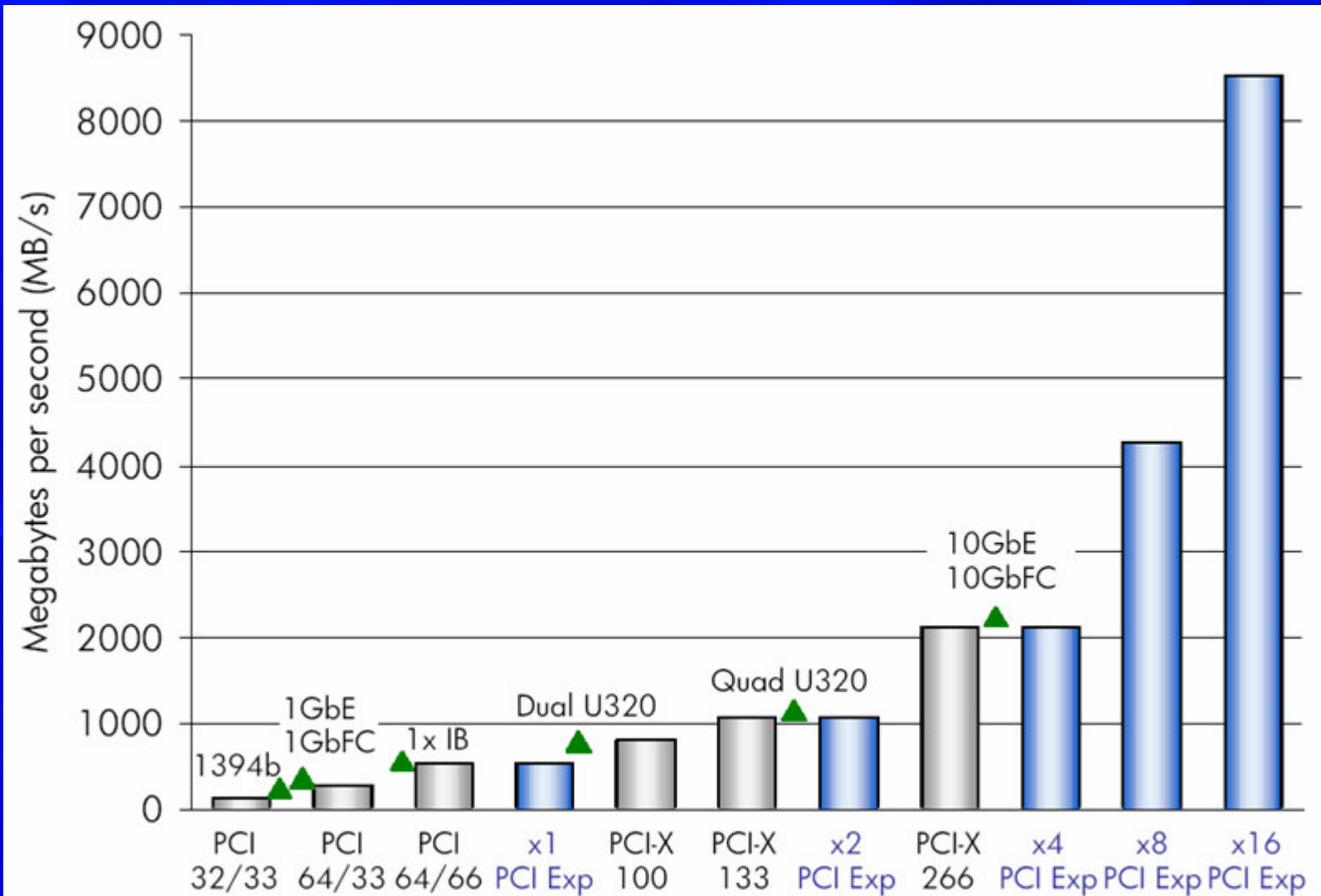
Two x8 Slots & No Bridge



- Board Area Reduced by 53%
- Board Layer Count Reduction Opportunity
- Component Count Decreases



# PCI-Express Bandwidth



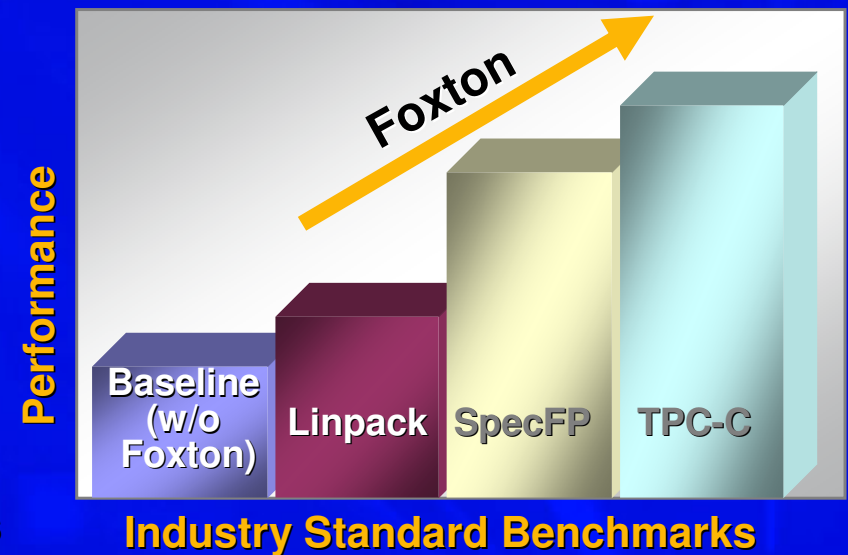
# Foxton Technology

## On-demand Performance Boost



- New processor feature boosting server performance dynamically based on application power consumption<sup>1</sup>
- Example:
  - Processor = 1.6 GHz
  - Processor with Foxton = 1.6GHz + up to 10% (depending on app)
- Largest performance boost on transaction based applications (databases, BI, ERP,...)
- No additional changes to OEM systems required

### Performance Boost with Foxton Technology



***Foxton delivers on-demand performance boost for greater productivity and efficiency***



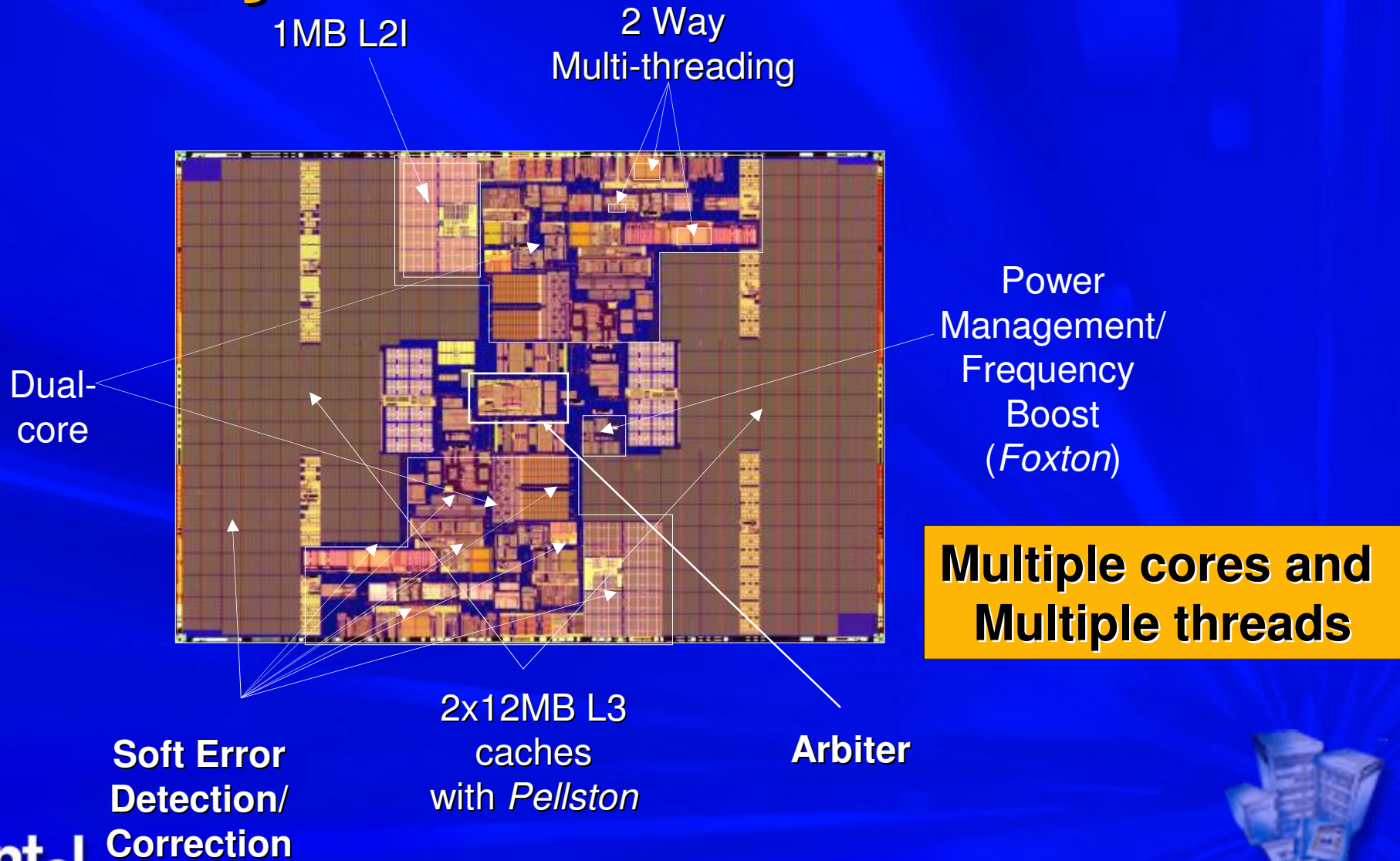
<sup>1</sup> Performance boost varies by application. Values are estimates

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# Why Pellston?





# Pellston Technology

## Cache Reliability

- **Benefits**
  - Automatically disables cache lines in the event of hard cache memory error
  - Removes impact of 2-bit ECC errors in L3 cache that have single bit hard failures
  - Allows processor and system to continue normal operation
- **How it works**
  - 1) Cache line access with error detected
  - 2) Cache line is tested for hard error
  - 3) If hard error is detected, cache line is disabled while processor and system continue normal operation

*Pellston helps improve reliability and uptime*



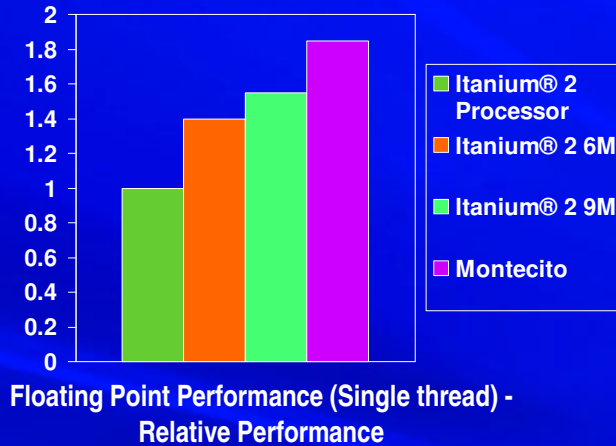
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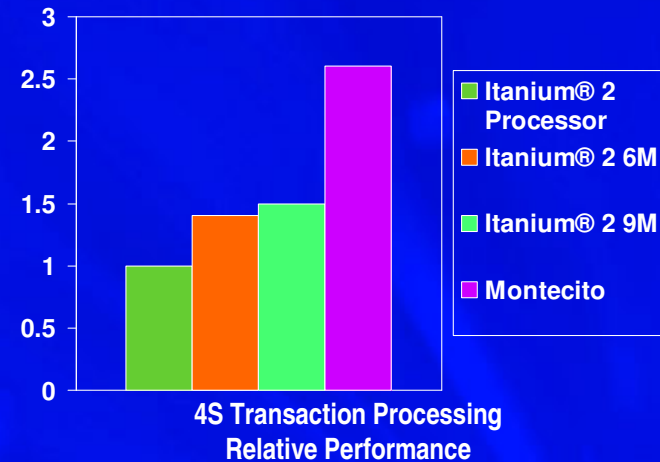
# Performance Innovations

- Intel® Itanium® 2 Processor Performance Strategy: increased performance/thread, then increased number of threads

## Increased Performance/Thread



## Multi-threaded Performance



- Driven by:
  - Increased frequency
  - Increased L3 cache
  - Increased bus speed

- Driven by:
  - Dual core Montecito
  - Multi-threading support in Montecito

**Montecito: 4 virtual processors**

Source: Intel Corporation  
All data measured at Intel on current processors. Projections on future processors based on Intel estimates using similar workload testing at Intel (Transaction processing using 64GB of memory, Floating point using 4GB).



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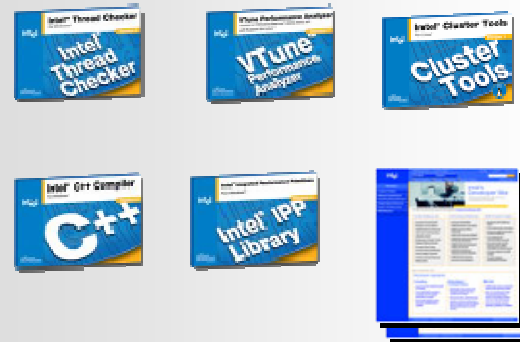
# Intel Enabling Resources

## Developer Platforms



HT/ Dual/Multi-Core Platforms  
Remote Access

## SW Tools and Expertise



Intel Compilers  
Intel Threading Toolkit,  
Performance Libraries,  
Whitepapers  
SW Engineers

## Extensive Support Services

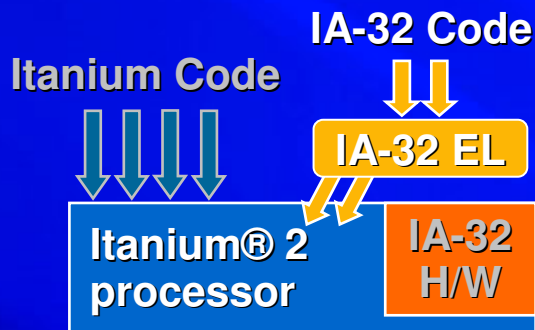
Early Access Program  
Intel Software College  
Application Tuning Centers  
Intel Solution Services

Helping Users and ISVs Optimize Solutions Performance



# IA-32 Execution Layer Functionality

- IA-32 Execution Layer (IA-32 EL) supports 32-bit applications running on Itanium® 2-based systems



- Historically, support for IA-32 applications has been carried out by on-die hardware
- Today, with supporting operating systems, 32-bit applications run using IA-32 EL
- IA-32 EL runs as part of the operating system and is transparent to the end user<sup>1</sup>

- IA-32 EL provides improved performance over on-die hardware<sup>2</sup>
  - Broadens the range of IA-32 applications that run well on Itanium architecture
  - Improves flexibility to add enhancements and support for new IA-32 instructions
  - Primary or performance-sensitive applications should be run on their native hardware platforms for optimal performance and capabilities

<sup>1</sup> IA-32 EL is turned on by default on some supporting operating systems but must be installed on some others. Once installed, no further end user intervention is required under normal operating conditions.

<sup>2</sup> Performance varies by application.

***IA-32 EL improves support for IA-32 applications running on Itanium® 2-based systems***



# Roadmaps



# Intel® Itanium® Processor Family Roadmap

## Leading Performance

4S+

**Itanium® 2**  
Processor (Madison 9M)  
1.6 GHz, 9M

**Montecito**  
Dual Core, 24MB  
Multi-threading

**Montvale**  
Dual Core,  
Multi-threading

**Tukwila**  
Multi-core

**Poulson**

## Leading \$/FLOPS

2S

**Itanium® 2**  
Processor (Fanwood)  
1.6 GHz, 3M, DP

**Millington**  
DP, Montecito-based

**DP Montvale**  
DP, Montvale-based

**Dimona**  
DP, Tukwila-based

**Future**  
DP, Poulson-based

## Lower Power

2S

**LV Itanium® 2**  
Processor (LV Fanwood)  
1.3 GHz, 3M, DP

**LV Millington**  
DP, Low Voltage,  
Montecito-based

**LV Montvale**  
DP, Low Voltage,  
Montvale-based

**LV Dimona**  
DP, Low Voltage,  
Tukwila-based

**Future**  
DP, Low Voltage,  
Poulson-based

## New Technologies

- Multi-core
- Multi-threading
- Dynamic performance boost (Foxton)
- Dynamic power management (DBS)
- Cache reliability (Pellston)
- Intel® Virtualization Technology
- Multi-core enhancements
- Enhanced RAS
- Enhanced virtualization
- Enhanced I/O & memory
- Common system architecture w/ Intel® Xeon™



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# Backup



# Building Success for Itanium® Architecture

Success Factor	Progress in '04
<b>Sales growth</b>	<ul style="list-style-type: none"> <li>☑ ~3X growth for Itanium 2-based systems in revenue<sup>1</sup></li> <li>☑ 1.8X growth for Itanium 2-based systems in units<sup>1</sup></li> <li>☑ MSS up 200% over 1 year, while RISC stayed flat<sup>1</sup></li> </ul>
<b>Adoption by business leaders</b>	<ul style="list-style-type: none"> <li>☑ Deployed by 70 of the Global 100, including 9 of the top 10<sup>2</sup></li> <li>☑ &gt;2.5X growth on Top 500* List of supercomputers in 1 year<sup>3</sup></li> <li>☑ 94% of surveyed customers with Itanium 2-based platforms plan to buy more<sup>4</sup></li> </ul>
<b>Support from industry leaders</b>	<ul style="list-style-type: none"> <li>☑ &gt;2X growth in applications<sup>2</sup></li> <li>☑ New platform releases or announcements</li> </ul>

***Itanium architecture made strong progress in '04 & momentum continues in '05***



<sup>1</sup> Source: IDC. 2/05

<sup>2</sup> Source: Intel 2/05

<sup>3</sup> Source: [www.top500.org/](http://www.top500.org/) as of 2/05

<sup>4</sup> Source: Forrester Research 2/05

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